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EXAMINER	
CHEN, ERIC BRICE	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,056	WILLE ET AL.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 6/24/03.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-49 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-49 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/24/03; 9/22/03. 1/7/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Applicant is advised of possible benefits under 35 U.S.C. 119(a)-(d), wherein an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1- 6, 11, 13-18, 24, 27, 29-30, and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Lui et al. (U.S. Patent No. 6,689,695).

4. As to claim 1, Lui discloses a method for forming an etched pattern on a semiconductor substrate, the method comprising the steps of: depositing a thin film (250) (column 5, lines 41-43) on the substrate (200) (Figure 2A); depositing a layer of planarizing material (270) (column 5, lines 54-60) on the thin film (250) (Figure 2B); depositing a layer of barrier material (280) on the layer of planarizing material (270) (column 6, lines 1-6); depositing at least one layer of imaging material (290) on the layer

of barrier material (280) (column 6, lines 6-7); forming at least one first pattern shape (295) in the layers of imaging material (290), barrier material (280) and planarizing material (270) (column 6, lines 13-15; lines 30-35); removing the imaging material (290), either after or concurrently with forming the first pattern shape (295) in the planarizing material (270) (Figure 2D); transferring the first pattern shape (295) to the thin film (250) (column 6, lines 30-35; Figure 2E); removing the barrier layer (280), either after or concurrently with transferring the first pattern shape (295) to the thin film (250) (Figure 2E); and removing the planarizing material (270) (column 6, lines 35-37; Figure 2F).

5. As to claim 2, Lui discloses that at least one second pattern shape (265) is formed in the thin film (250) prior to depositing the layer of planarizing material (270) (column 5, lines 48-52), and the second pattern shape (265) is filled by the planarizing material (270) (column 5, lines 54-60).

6. As to claim 3, Lui discloses that the thin film (250) is a dielectric material (column 5, lines 41-43).

7. As to claim 4, Lui discloses that the thin film (250) is a low-k dielectric material (column 5, lines 41-43).

8. As to claim 5, Lui discloses that the low-k dielectric material has a dielectric constant less than 3.9 (column 5, lines 3-5).

9. As to claim 6, Lui discloses that the low-k dielectric material has a dielectric constant less than about 3.2 (column 5, lines 15-19).

10. As to claim 11, Lui discloses that the barrier material (280) comprises a material selected from the group consisting of silicon, silicon nitride, silicon carbide, titanium nitride, and tantalum nitride (column 6, lines 2-4).

11. As to claim 13, Lui discloses that the step of filling the first pattern shape (295) with a conductive material, after removing the imaging material (290), the barrier material (280) and the planarizing material (270) (column 6, lines 37-39).

12. As to claim 14, Lui discloses that the conductive material comprises copper (column 6, lines 37-39; column 4, lines 65-66)

13. As to claim 15, Lui discloses a method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of: depositing a dielectric material (250) (column 5, lines 41-43) on the substrate (200) (Figure 2A); forming at least one via (265) in said dielectric material (250) (column 5, lines 48-52), such that at least one of the vias is positioned over the patterned conductor (210) (column 4, lines 61-62; Figure 2A); depositing a layer of planarizing material (270) on the dielectric material (250) and in the via (265) (column 5, lines 54-60; Figure 2A); depositing a layer of barrier material (280) on the layer of planarizing material (270) (column 6, lines 1-6); depositing at least one layer of imaging material (290) on the layer of barrier material (280) (column 6, lines 6-7); forming at least one trench (295) in the layers of imaging material (290), barrier material (280) and planarizing material (270) (column 6, lines 13-15; lines 30-35), such that at least one of the trenches (295) is positioned over the via (265) (Figure 2D); removing the imaging material (290), either after or concurrently with forming the trench

(295) in the planarizing material (270) (Figure 2D); transferring the at least one trench to the dielectric material (250), such that at least one of the trenches (295) is positioned over the via (265) (Figure 2E); removing the barrier material (280), either after or concurrently with transferring the at least one trench (295) to the dielectric material (250) (Figure 2D); and removing the planarizing material (270) (column 6, lines 35-37; Figure 2F).

14. As to claim 16, Lui discloses that the dielectric material (250) is a low-k dielectric material (column 5, lines 41-43).

15. As to claim 17, Lui discloses that the low-k dielectric material has a dielectric constant less than 3.9 (column 5, lines 3-5).

16. As to claim 18, Lui discloses that the low-k dielectric material has a dielectric constant less than about 3.2 (column 5, lines 15-19).

17. As to claim 24, Lui discloses the barrier material (280) is silicon dioxide (column 6, lines 2-4).

18. As to claim 27, Lui discloses that the barrier material (280) comprises a material selected from the group consisting of silicon, silicon nitride, silicon carbide, titanium nitride, and tantalum nitride (column 6, lines 2-4).

19. As to claim 29, Lui discloses the step of filling the via (265) and the trench (295) with a conductive material, after removing the imaging material (290), the barrier material (280) and the planarizing material (270) (column 6, lines 37-39).

20. As to claim 30, Lui discloses that the conductive material comprises copper (column 6, lines 37-39; column 4, lines 65-66).

21. As to claim 31, Lui discloses that at least one via (265) has a height, and the layer of planarizing material (270) has a thickness of about half the via height to about twice the via height. From Figure 2A, the height of via (265) ranges from 421 nm to 1,400 nm (total thicknesses of layers (230), (240), (250), and (260)). The thickness of layer (230) ranges from 200 to 600 nm (column 5, lines 13-15). The thickness of layer (240) ranges from 1 to 100 nm (column 5, lines 35-37). The thickness of layer (250) ranges from 200 to 600 nm (column 5, lines 41-43). The thickness of layer (260) ranges from 20 to 100 nm (column 5, lines 43-45). The height of planarizing material (270) ranges from 100 to 500 nm (column 5, lines 57-59).

22. As to claim 32, Lui discloses that the layer of barrier material (280) has a thickness of about 50 to 100 nm (column 6, lines 2-6).

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

25. Claims 7-8, 12, 20-23, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lui in view of Bao et al. (U.S. Patent Appl. Pub. No. 2004/008764).

26. As to claims 7 and 20, Lui does not expressly disclose that the planarizing material is a poly(hydroxystyrene)-based system. However, Bao discloses a method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of: depositing a dielectric material (54) on the substrate (50) (paragraph 0029; Figure 2A); forming at least one via (57) in said dielectric material (54) (paragraph 0031), such that at least one of the vias is positioned over the patterned conductor (51) (Figure 2A); depositing a layer of planarizing material (58) on the dielectric material (54) and in the via (57) (paragraph 0031). Furthermore, Bao teaches, the resin serves an inert plug for the via and prevents amines from the photoresist from diffusing into the dual damascene structure (paragraph 0019). Poly(hydroxystyrene)-based compounds are commonly used resins. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lui's methods with the teachings of Bao (planarizing material is a resin, such as a poly(hydroxystyrene)-based compound). One who is skilled in the art would be motivated to use an inert resin material in order to prevent the interdiffusion of amines from the photoresist.

27. As to claim 8 and 23, Lui does not disclose that planarizing material is selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters. However, Bao teaches that inert resins can be used as a planarizing material (paragraph 0031). Polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters are commonly used resin materials. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select such resins to be used as a planarizing material. One who is skilled in the art would be motivated to use an inert resin material in order to prevent the interdiffusion of amines from the photoresist.

28. As to claims 12 and 28, Lui does not expressly disclose the steps of: depositing a layer of anti-reflective coating on the barrier material, prior to depositing the layer of imaging material; and removing the anti-reflective coating, either after or concurrently with forming the first pattern shape in the planarizing material. However, Bao disclose the steps of: depositing a layer of anti-reflective coating (62) on the barrier material (60), prior to depositing the layer of imaging material (64) (paragraph 0032); and removing the anti-reflective coating (62), either after or concurrently with forming the first pattern shape (or via) (66) in the planarizing material (58) (paragraph 0039). Bao teaches that variable reflectivity of the exposing radiation off the substrate must be controlled in order to achieve the feature size specification. One widely used technique

is to form an anti-reflective coating on the substrate before coating the photoresist film (paragraph 0007). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lui's method with the teachings of Bao (depositing a layer of anti-reflective coating on the barrier material). One who is skilled in the art would be motivated to incorporate an anti-reflective coating under the imaging layer to improve resolution of the lithography step.

29. As to claim 21, Lui does not expressly disclose the step of baking the planarizing material at a temperature of about 200°C to about 250°C, after deposition of the planarizing material. However, Bao discloses the step of baking the planarizing material (58) at a temperature of about 200°C to about 250°C, after deposition of the planarizing material (58) (paragraph 0031). Boa teaches the baking the planarizing material cures the resin and prevents outgassing during the processing of overlying layers (paragraph 0031). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the step of baking the planarizing material at a temperature of about 200°C to about 250°C. One who is skilled in the art would be motivated cures the resin and prevents outgassing during the processing of overlying layers.

30. As to claim 22, Lui does not disclose the step of baking the planarizing material at a temperature of about 225°C, after deposition of the planarizing material. However, Bao discloses the step of baking the planarizing material (58) at a temperature of about 225°C, after deposition of the planarizing material (58) (paragraph 0031).

31. Claims 9-10, 19, and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lui in view of Wolf.

32. As to claims 9 and 25, Lui discloses that barrier material (280) comprises silicon dioxide (column 6, lines 2-6), but does not expressly disclose that the silicon oxide is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100°C to about 225°C. Wolf teaches that chemical vapor deposition is a common method of depositing silicon dioxide (vol. 1, pages 182-83) and that a typical deposition temperature for plasma-enhanced chemical vapor deposition is 200°C (vol. 1, Table 2, page 183). It should be noted that the applicants' temperature range overlaps with the typical temperature taught by Wolf. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lui's method with the teachings of Wolf (silicon oxide is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100°C to about 225°C). One who is skilled in the art would be motivated to select an established method for depositing oxide and to select deposition temperatures that either overlap or are similar to conventional temperatures.

33. As to claims 10 and 26, Lui discloses that barrier material (280) comprises silicon dioxide (column 6, lines 2-6), but does not expressly disclose that the silicon oxide is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150°C. Wolf teaches that chemical vapor deposition is a common method of depositing silicon dioxide (vol. 1, pages 182-83) and that a typical deposition temperature for plasma-enhanced chemical vapor deposition is 200°C (vol. 1, Table 2, page 183).

Although applicants' temperature range is outside the typical temperature taught by Wolf, the temperatures are close enough, such that similar results would be expected. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lui's method with the teachings of Wolf (silicon oxide is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150°C). One who is skilled in the art would be motivated to select an established method for depositing oxide and to select a deposition temperature that is similar to a conventional temperature.

34. As to claim 19, Lui does not expressly disclose that the low-k dielectric material is SiCOH deposited by chemical vapor deposition. However, Wolf teaches that SiCOH, deposited by chemical vapor deposition, is a commonly used low-k dielectric material (vol. 4, page 690) for damascene structures (vol. 4, page 689). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lui's method with the teachings of Wolf (the low-k dielectric material is SiCOH deposited by chemical vapor deposition). One who is skilled in the art would be motivated to use a commonly used low-k material, which has been successfully implemented for producing damascene structures.

35. Claims 33-36, 42, 45, and 47-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Daniels et al. (U.S. Patent No. 6,583,047).

36. As to claim 33, Daniels discloses a method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of: depositing a dielectric material on the

substrate (column 15, lines 58-61; Figure 3A); forming at least one trench in the dielectric material (column 15, lines 65-67; column 16, lines 1-2), such that at least one of the trenches is positioned over the patterned conductor (column 14, lines 39-40; lines 47-48); depositing a layer of planarizing material on the dielectric material and in the trench (column 16, lines 3-6; Figure 3D); depositing at least one layer of imaging material on the layer of planarizing material (column 16, lines 6-9; Figure 3E); forming at least one via in the layers of imaging material and planarizing material (column 16, lines 11-13), such that at least one of the vias is positioned over the trench (Figure 3F) and the patterned conductor (column 14, lines 39-40); removing the imaging material, either after or concurrently with forming the via in the planarizing material (column 16, lines 13-16; Figure 3G); transferring the at least one via to the dielectric material (Figure 3F), such that at least one of the vias is positioned over the trench and the patterned conductor (column 14, lines 39-40; lines 47-48); and removing the planarizing material (column 16, lines 13-16; Figure 3F). Daniels does not expressly disclose the steps of: depositing a layer of barrier material on the layer of planarizing material; depositing at least one layer of imaging material on the layer of barrier material; forming at least one via in the barrier material; and removing the barrier material, either after or concurrently with transferring the at least one via to the dielectric material. However, in a separate embodiment, Daniels teaches that a barrier material may be formed between the photoresist and dielectric (column 17, lines 65-67; column 21, lines 10-12), to prevent adverse reactions between the two layers (column 1, lines 51-62). Therefore, it would have been obvious to one of ordinary skill in the art to deposit a layer of barrier material

under the photoresist layer and adapt the process steps to include the barrier material layer. One who is skilled in the art would be motivated to deposit a layer of barrier material under the photoresist layer in order to prevent the occurrence of adverse reactions between layers.

37. As to claim 34, Daniels discloses that the dielectric material is a low-k dielectric material (column 10, lines 56-58).

38. As to claim 35, Daniels discloses that the low-k dielectric material has a dielectric constant less than 3.9 (column 10, lines 58-63).

39. As to claim 36, Daniels discloses that the low-k dielectric material has a dielectric constant less than about 3.2 (column 10, lines 58-63).

40. As to claim 42, Daniels discloses that the barrier material is silicon dioxide (column 17, line 67; column 18, line 1).

41. As to claim 45, Daniels discloses that the barrier material comprises a material selected from the group consisting of silicon, silicon nitride, silicon carbide, titanium nitride, and tantalum nitride (column 17, lines 65-67; column 18, lines 1-8).

42. As to claim 47, Daniels discloses that step of filling the via and the trench with a conductive material, after removing the imaging material, the barrier material and the planarizing material (column 16, lines 16-19).

43. As to claim 48, Daniels discloses that the conductive material comprises copper (column 10, lines 44-46).

44. As to claim 49, Daniels discloses that the layer of barrier material has a thickness of about 50 to 100 nm (column 21, lines 10-12; lines 28-30).

45. Claims 37 and 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Daniels in view of in view of Wolf.

46. As to claim 37, Daniels does not expressly disclose that the low-k dielectric material is SiCOH deposited by chemical vapor deposition. However, Wolf teaches that SiCOH, deposited by chemical vapor deposition, is a commonly used low-k dielectric material (vol. 4, page 690) for damascene structures (vol. 4, page 689). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Daniels' method with the teachings of Wolf (the low-k dielectric material is SiCOH deposited by chemical vapor deposition). One who is skilled in the art would be motivated to use a commonly used low-k material, which has been successfully implemented for producing damascene structures.

47. As to claim 43, Daniels does not expressly disclose that the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100°C to about 225°C. Wolf teaches that chemical vapor deposition is a common method of depositing silicon dioxide (vol. 1, pages 182-83) and that a typical deposition temperature for plasma-enhanced chemical vapor deposition is 200°C (vol. 1, Table 2, page 183). It should be noted that the applicants' temperature range overlaps with the typical temperature taught by Wolf. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Daniels' method with the teachings of Wolf (silicon oxide is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100°C to about 225°C). One who is skilled in the art would be motivated to select an established method for depositing oxide and

to select deposition temperatures that either overlap or are similar to conventional temperatures.

48. As to claim 44, Daniels does not expressly disclose that the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150°C. Wolf teaches that chemical vapor deposition is a common method of depositing silicon dioxide (vol. 1, pages 182-83) and that a typical deposition temperature for plasma-enhanced chemical vapor deposition is 200°C (vol. 1, Table 2, page 183). Although applicants' temperature range is outside the typical temperature taught by Wolf, the temperatures are close enough, such that similar results would be expected. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Daniels' method with the teachings of Wolf (silicon oxide is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150°C). One who is skilled in the art would be motivated to select an established method for depositing oxide and to select a deposition temperature that is similar to a conventional temperature.

49. Claims 38-41, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Daniels in view of Wolf, in further view of Bao.

50. As to claim 38, Daniels does not expressly disclose that the planarizing material is a poly(hydroxystyrene)-based system. However, Bao discloses a method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of: depositing a dielectric material (54) on the substrate (50) (paragraph 0029; Figure 2A); forming at

least one via (57) in said dielectric material (54) (paragraph 0031), such that at least one of the vias is positioned over the patterned conductor (51) (Figure 2A); depositing a layer of planarizing material (58) on the dielectric material (54) and in the via (57) (paragraph 0031). Furthermore, Bao teaches, the resin serves an inert plug for the opening and prevents amines from the photoresist from diffusing into the dual damascene structure (paragraph 0019). Poly(hydroxystyrene)-based compounds are commonly used resins. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Daniels' methods with the teachings of Bao (planarizing material is a resin, such as a poly(hydroxystyrene)-based compound). One who is skilled in the art would be motivated to use an inert resin material in order to prevent the interdiffusion of amines from the photoresist.

51. As to claim 39, Daniels does not expressly disclose the step of baking the planarizing material at a temperature of about 200°C to about 250°C, after deposition of the planarizing material. However, Bao discloses the step of baking the planarizing material (58) at a temperature of about 200°C to about 250°C, after deposition of the planarizing material (58) (paragraph 0031). Boa teaches the baking the planarizing material cures the resin and prevents outgassing during the processing of overlying layers (paragraph 0031). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the step of baking the planarizing material at a temperature of about 200°C to about 250°C. One who is skilled in the art would be motivated cures the resin and prevents outgassing during the processing of overlying layers.

52. As to claim 40, Daniels does not expressly disclose the step of baking the planarizing material at a temperature of about 225°C, after deposition of the planarizing material. However, Bao discloses the step of baking the planarizing material (58) at a temperature of about 225°C, after deposition of the planarizing material (58) (paragraph 0031).

53. As to claim 41, Daniels does not disclose that planarizing material is selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters. However, Bao teaches that inert resins can be used as a planarizing material (paragraph 0031). Polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters are commonly used resin materials. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select such resins to be used as a planarizing material. One who is skilled in the art would be motivated to use an inert resin material in order to prevent the interdiffusion of amines from the photoresist.

54. As to claim 46, Daniels does not expressly disclose the steps of: depositing a layer of anti-reflective coating on the barrier material, prior to depositing the layer of imaging material; and removing the anti-reflective coating, either after or concurrently with forming the via in the planarizing material. However, Bao disclose the steps of: depositing a layer of anti-reflective coating (62) on the barrier material (60), prior to

depositing the layer of imaging material (64) (paragraph 0032); and removing the anti-reflective coating (62), either after or concurrently with forming the first pattern shape (66) in the planarizing material (58) (paragraph 0039). Bao teaches that variable reflectivity of the exposing radiation off the substrate must be controlled in order to achieve the feature size specification. One widely used technique is to form an anti-reflective coating on the substrate before coating the photoresist film (paragraph 0007). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Daniels' method with the teachings of Bao (depositing a layer of anti-reflective coating on the barrier material). One who is skilled in the art would be motivated to incorporate an anti-reflective coating under the imaging layer to improve resolution of the lithography step.

Conclusion

55. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wu et al. (U.S. Patent No. 6,720,256) discloses forming a dual damascene structure in which an inert resin is inserted into a via to prevent poisoning. Fujimoto et al. (U.S. Patent No. 6,835,652) discloses embedding a via hole opening with a protective film and resin. Hussein et al. (U.S. Patent No. 6,365,529) discloses forming a dual damascene structure in which a via is filled with a sacrificial material. Kim et al. (U.S. Patent Appl. Pub. No. 2004/0018721) discloses forming a dual damascene structure in which the primary opening is filled with a sacrificial material with a low dielectric constant.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Jan. 26, 2005

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